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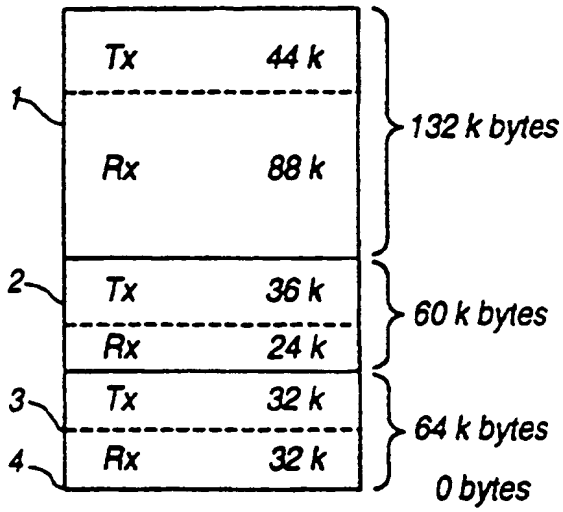
(54) **Adjustable fifo-based memory scheme**

(57) A large FIFO memory device has its total available memory capacity partitioned into memory sections. The partitions are in the form of programmable delimiters in order to determine flexibly the size of the memory sections.



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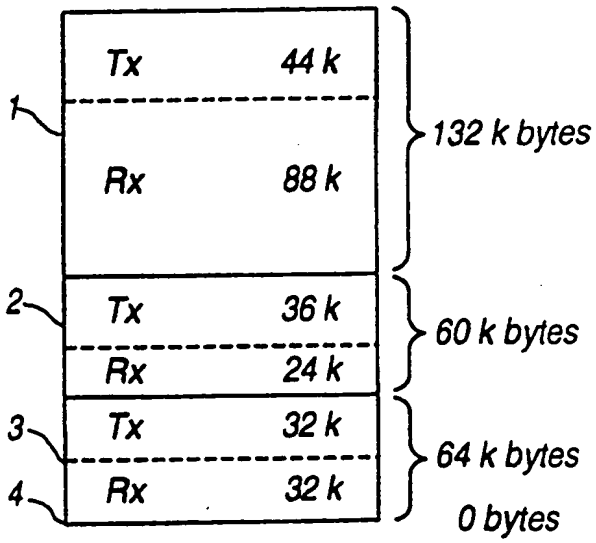
(57) Abstract

A large FIFO memory device has its total available memory capacity partitioned into memory sections. The partitions are in the form of programmable delimiters in order to determine flexibly the size of the memory sections.



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ADJUSTABLE FIFO-BASED MEMORY SCHEME

The present invention relates to first in first out (FIFO) memory devices and more particularly to a method and apparatus for altering the boundaries of sections of a memory device whereby data is stored in a FIFO structure.

One use of the FIFO memory devices is in the field of computer networks where each port of the network has associated with it a section of memory. Customarily, the amount of memory associated with each port is fixed and the total amount is also shared in a fixed relationship between transmission and reception.

This can result in large amounts of memory being required which is inefficient and leads to undue expense.

The present invention proposes to provide programmable delimiters for a FIFO based memory device in order to determine flexibly the total amount of memory allocated to a port as well as the amount of memory allocated for transmission separately from the amount of memory allocated for reception at that port.

In order that the present invention be more readily understood, an embodiment thereof will now be described by way of example with reference to the accompanying drawing, in which:-

Fig. 1 shows diagrammatically a conventional FIFO memory arrangement;

Fig. 2 shows diagrammatically a FIFO memory arrangement according to the present invention; and

Figs. 3a and 3b are diagrams to explain the operation of a FIFO according to the present invention.

A first in first out memory device is a well known memory arrangement which operates in the manner one would expect given its description. Data is

written into the memory in a particular order and is read from the memory in the same order as it was written. In conventional network arrangements, each port is allocated a fixed amount of FIFO memory e.g. 64K bytes with in this example 32k bytes allocated for transmission and 32k bytes allocated to reception. As is apparent from Fig. 1 of the accompanying drawing, the memory associated with more than one port is provided in a single memory device. In the drawing, memory associated with 4 ports is shown.

The present invention proposes to adjust the position of the boundaries between the sections of memory. This is achieved by altering the address of the delimiters representing the beginning and end of each section of memory. By altering the delimiter addresses, one can vary the size of memory associated with each port as well as the relative sizes of the transmission and reception portions of memory associated with each port.

Fig. 2 shows diagrammatically how a FIFO memory could be partitioned according to the present invention. Here one assumes that there are four ports as before and that the total available memory is unaltered at 256K bytes. These numbers were chosen at random for the sake of example only.

It will be noted that port 4 according to this example has not been allocated any memory at all i.e. it is an unused port. Port 3 has been allocated 64K bytes divided equally between transmission and reception while port 2 has been allocated 60K bytes with more memory being allocated for transmissions than for receptions. Port 1 is allocated all the remaining memory with more allocated for reception than transmission. With this additional memory allocation, port 1 could, for example be used as an ethernet port with 100 MHz bandwidth while the other ports are normal 10 MHz ports.

The amount of memory associated with each port and the relative amounts of transmission and reception memory can be determined beforehand on the basis of likely traffic flows and then fixed. Alternatively, one can monitor the traffic associated with each of the ports and on the basis of actual traffic flows

adaptively adjust the positions of the delimiters, depending on the actual statistics of the transfer through the system.

In more detail, it will be understood that the size i.e. the number of bits in the words used for the delimiters is conditioned upon the maximum size of the memory as well as the size of the units of memory. For example, the delimiter could be used to allocate memory in blocks of 8K bytes so that with a total memory capability of 256K bytes a word of length 6 bits would be required for the pointer, whereas if the blocks were of 2K bytes then 8 bits would be required, or for full granularity blocks of 1 byte will require 18 bits.

Referring now to Figs. 3a and 3b these are diagrams which will be used to describe the operation of the present invention. A FIFO 30 has an area of memory 31 defined by a bottom delimiter A and a top delimiter B, it being assumed that data enters at the top. As data is stored in the FIFO, a top pointer rises through the memory and as data is read from the memory a bottom pointer also rises through the memory. The positions of the pointers at one point in time are shown in Fig. 3a. Eventually, the top pointer will reach the top delimiter B. If the memory is not full i.e. if data is being read out, the bottom pointer will have risen off the bottom delimiter A and so the top pointer will now start again at the bottom delimiter A and rise through the memory in a circulating fashion as will the bottom pointer. This situation is represented in Fig. 3b which represents the pointers at another point in time.

If we now consider the effect of altering the delimiters A and/or B in order to alter the size of the memory 31, it will be understood that some control of the delimiter alteration is required. When a new delimiter is introduced it is possible in some circumstances to delete any data in the memory 31 and introduce the new delimiter. However, it is preferable to alter delimiters only when it is safe to do so or in a manner that no data is lost.

One way of controlling the alteration of delimiters is to monitor the relative position of the top and bottom pointers and only alter the top delimiter B

when the top pointer is above the bottom pointer. The bottom delimiter can be altered as long as the bottom pointer is not at either the old or new bottom delimiter.

It will be appreciated that this process will allow very efficient use of the available memory which will save the amount of memory required as well as possibly allowing adaptive alteration of memory in existing networks to the existing traffic on the network.

CLAIMS:

1. A method for partitioning a finite memory into a plurality of sections, in each of which a separate FIFO queue operates, the method comprising moving partitions defining the sections so as to allocate amounts of the finite memory to each of said sections in accordance with the memory usage in each of said sections.

2. A method according to claim 1, in which a partition between two sections is moveable only when the memory immediately either side of the partition is not being used in a FIFO queue, and said partition is not permitted to pass a top or bottom pointer of a FIFO queue.

3. A method according to either of claims 1 or 2, for use in a switch attached to a computer network.

4. Apparatus for operating a plurality of FIFO queues comprising,

a finite memory means arranged to be partitioned into a plurality of sections, each containing one of said FIFO queues,

means for moving partitions defining said sections so as to allocate amounts of the finite memory means to each of said sections in accordance with the memory usage in each of said sections.

5. Apparatus according to claim 4, wherein said means for moving said partitions only allows movement of one of said partitions when the memory immediately either side of the partition is not being used in a FIFO queue, and does not allow movement of the partitions beyond a top or bottom pointer of a FIFO queue.

6. Apparatus according to claim 4 or 5, wherein said apparatus is for use in a switch attached to a computer network.

7. Apparatus for operating a plurality of FIFO queues, substantially as described herein with reference to the accompanying drawings.

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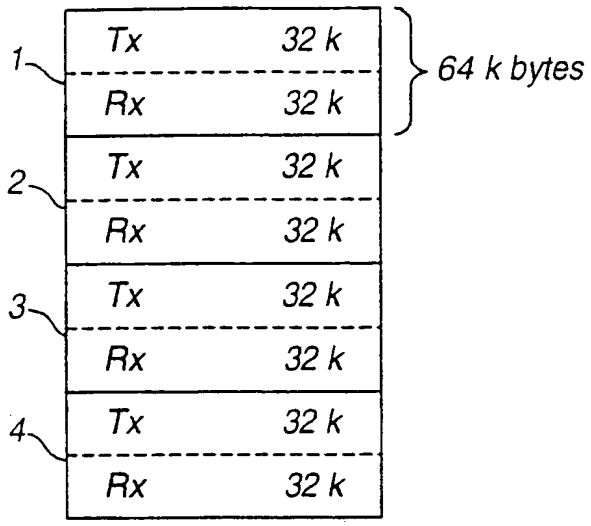

Fig. 1

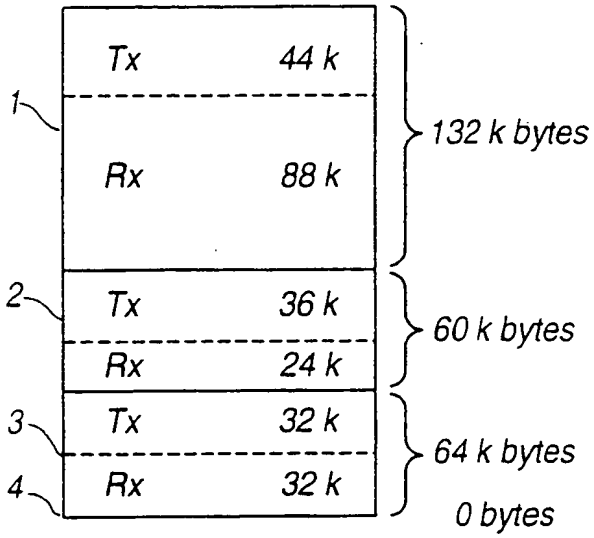

Fig. 2

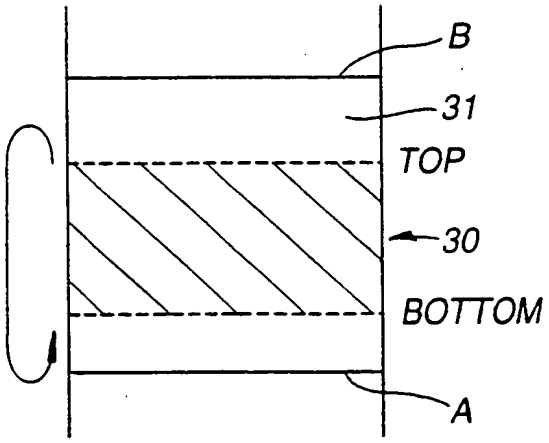

Fig.3a

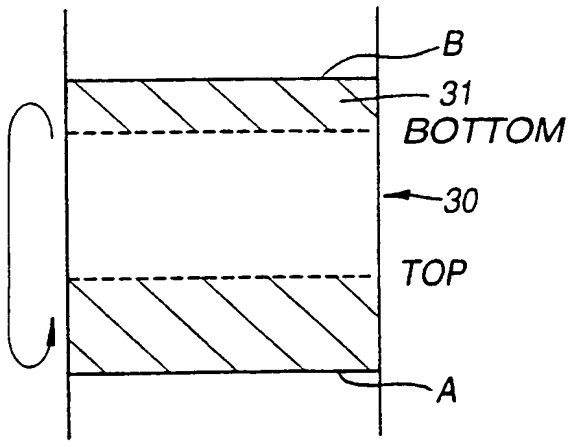

Fig.3b

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F5/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	COMPUTER DESIGN, vol. 32, no. 6, 1 June 1993, page 34, 36 XP000377572 "SPECIALTY SRAM COMBINES BEST OF DUAL-PORT SRAMS AND FIFOS" see page 36, column 1, line 8-57; figure 1	1-6

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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Name and mailing address of the ISA	Authorized officer
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